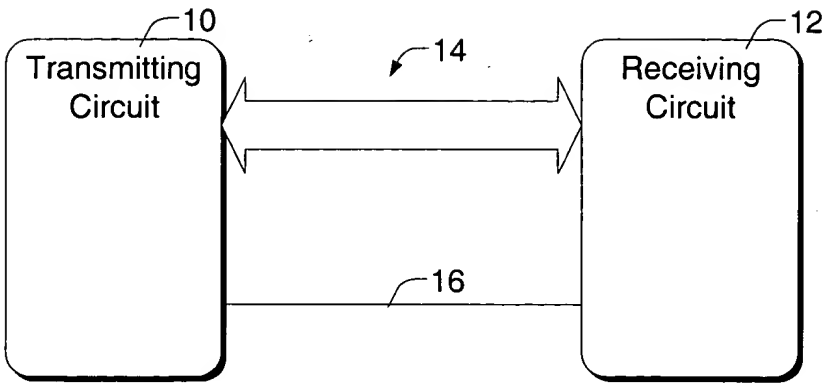


Fig. 1

Prior Art

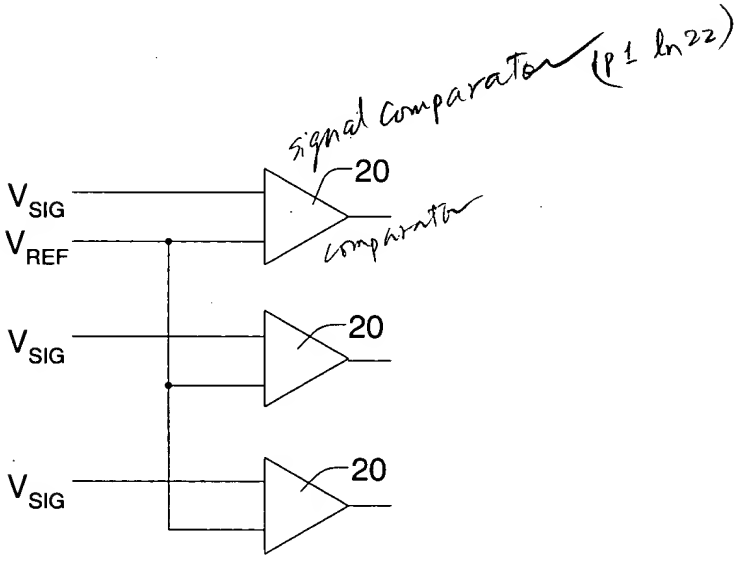


Fig. 2

Prior Art

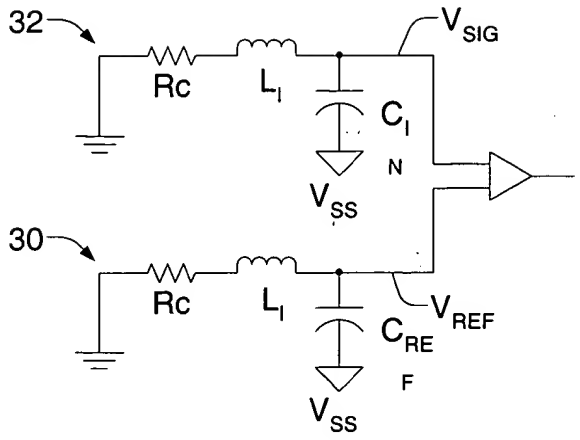


Fig. 3

Prior Art

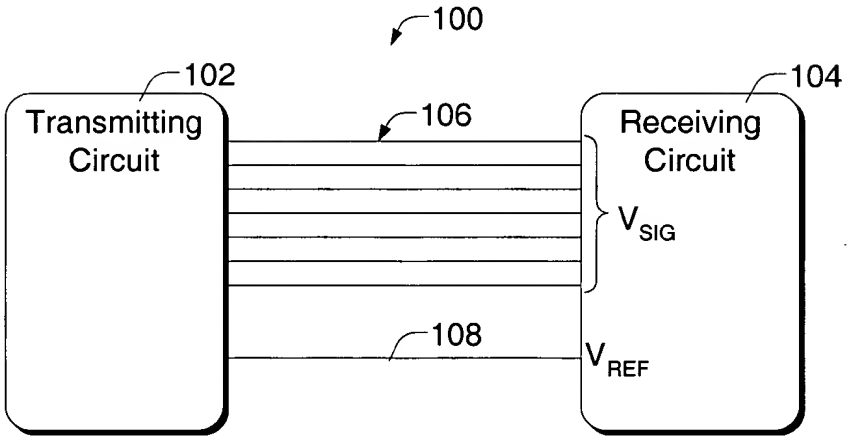


Fig. 4

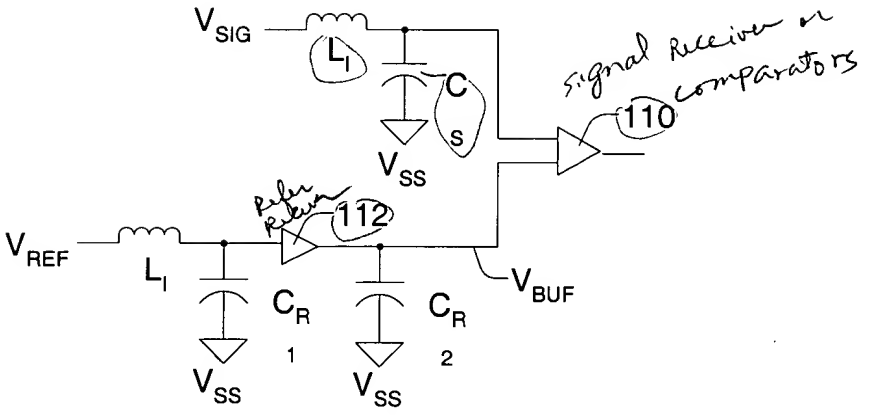


Fig. 5

Receiver circuitry

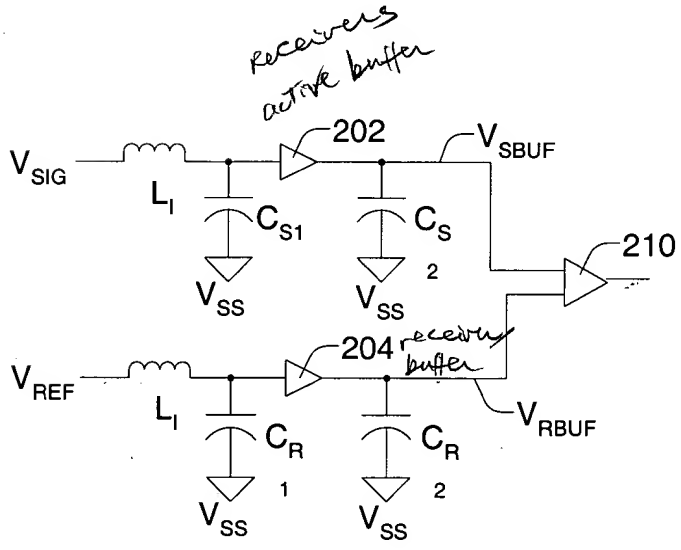


Fig. 6

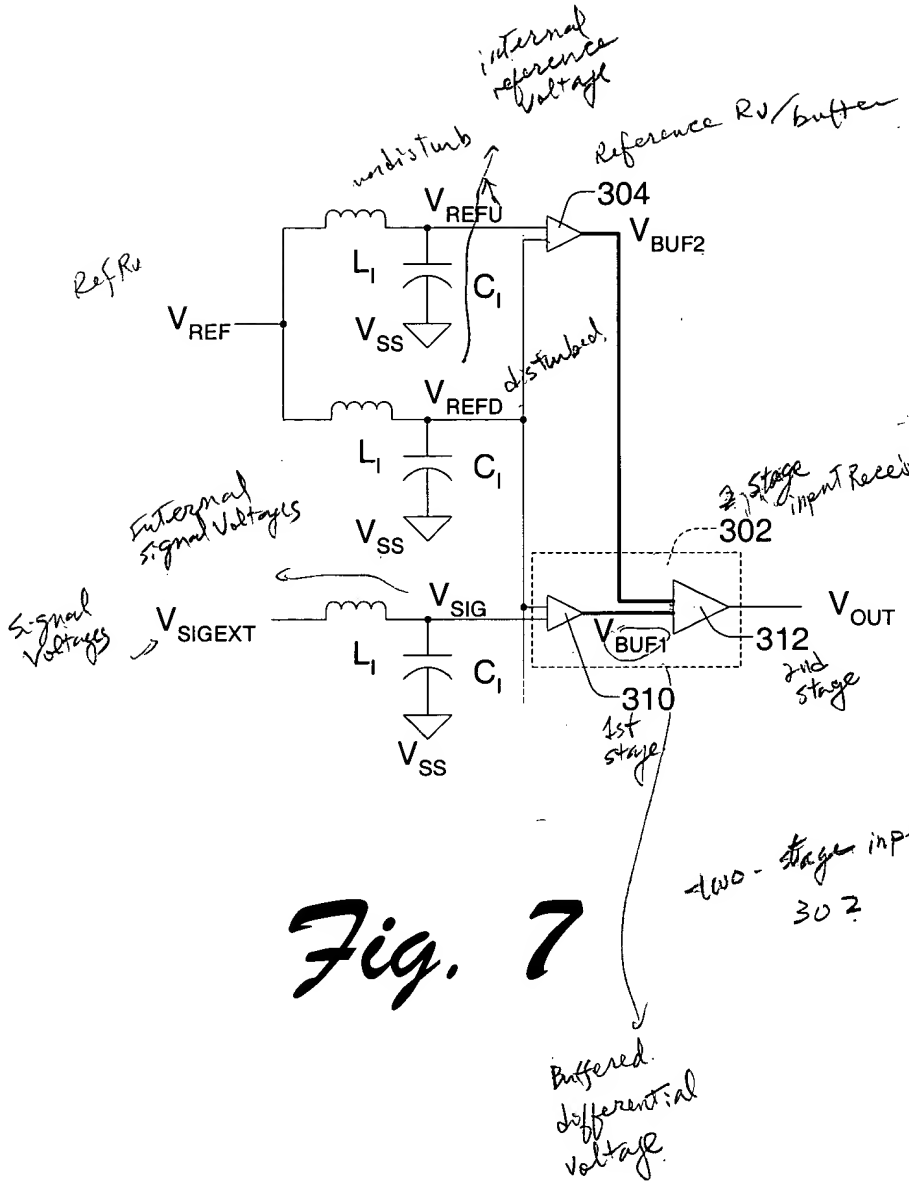
internal reference voltage
Reference RV/buffer
304
$V_{REFU}$
$V_{BUF2}$
$L_I$
$C_I$
$V_{SS}$
$V_{REF}$
$V_{REFD}$
distributed
2 stage input Receiver
302
External signal Voltages
$V_{SIG}$
$V_{SIGEXT}$
$V_{BUF1}$
$V_{OUT}$
312
2nd stage
310
1st stage
two-stage input receiver 302
Buffered differential voltage

Fig. 7